STUDER A812/A820
TLS-4000 MKII

INTERFACE DOCUMENTATION

Interface number : 1.812.409.20
IF - Doc number : 10.27.3170

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Order No.: 10.27.3170 (Ed. 0293)

Summary

1 General Information

1.1 Ordering Information

	Order number
■ Interface Set (including Interface, Cable and Documentation)	21.812.409.20
■ Interface Board (Hardware/Software)	1.812.409.20
■ Hardware: TLS Serial Interface	1.812.490.20
■ Software Set	1.812.923.20
■ IF-Cable 5m	1.023.778.00
■ Interface Docu-number	10.27.3170
■ Hardware (serial IF) Docu-number	10.27.3050

1.2 Slave Model

STUDER A820-2, A812 (TC versions)

1.3 Software

■ First release (index 20)	1.812.923.20 (41/92)

2 Installing Procedures

2.1 TLS 4000 Requirements

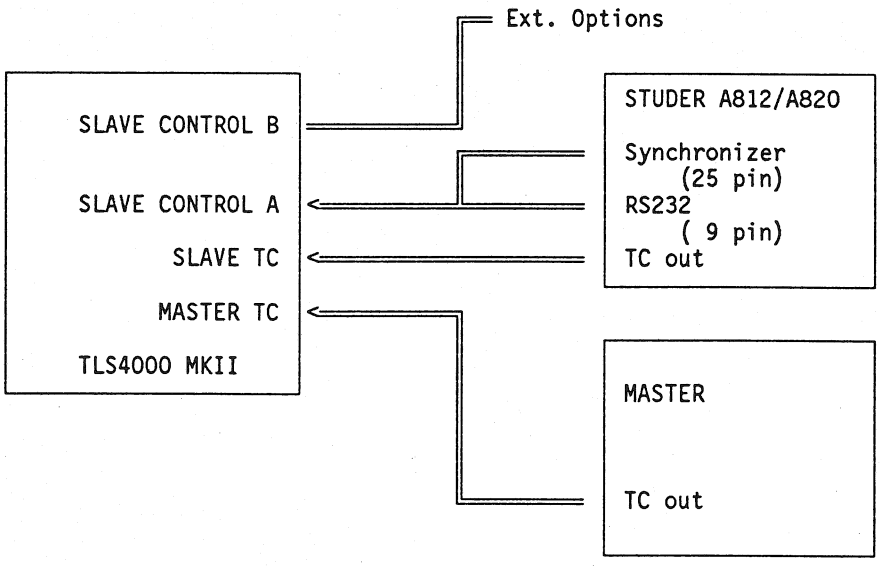
Order number

- Synchronizer Board 1.812.320.23 or later
- Interface: correct setup of the DIL-SWITCHES (see section 3.3)

2.2 Slave Requirements

- "no echo mode" set from menu;
- A820 software
  Master: 06/89 (and corresponding tape deck software)
- A812 software
  Master: 11/91 (and corresponding tape deck software)

2.3 Connection Slave-Synchronizer



2.4 Quick Test, Adjustments

Insert the Interface after switching off the synchronizer. Connect the slave machine and switch on synchronizer and slave.
During the first 5 seconds the interface will perform a short selftest. The result is commented with some led messages. If no errors have been found, the display is available for operation messages (see section 3.5)

The correct wiring of movepulse information may easily be checked by disconnecting the slave timecode cable. The time display on the LCU or a controller should be updated with correct speed and direction.

A good timecode on tape is essential for synchronizer operation and should be checked for master and slave.

No adjustments are necessary.

3 Operating Instructions

3.1 Technical Specifications

- Slave type:
  - Audio tape recorder;
  - SMPTE/EBU timecode with move information, no capstan tacho:
  - GOTO function with PLAY–STOP sequence;
  - Chase–Stop waiting in advance;
  - Transition Chase to Playsync direct.
- Tapedeck Control:
  - by serial communication, STUDER RS 232 protocol.
- Capstan control:
  - nom 9600 Hz, max 1.5 nom, min 0.66 nom.
- Movepulse information:
  - direction: LOW = rewind

  clock frequency for A812: 64 Hz @ 7.5 ips
  128 Hz @ 15 ips
  256 Hz @ 30 ips

  clock frequency for A820: 256 Hz @ 7.5 ips
  512 Hz @ 15 ips
  1024 Hz @ 30 ips
- Compensation of Record Dropin/out Delays:
  - compensated by synchronizer (includes transmission delays).
- Sync accuracy: typical 50 usec.
- Park accuracy: typical 20 msec. (GOTO function)
- Wow & Flutter: within slave specifications.
- Lock time:

  (in CUED status, Master Start - SYNC) : typical < 3 sec
  (in CHASE 10*vnom, Master Start - SYNC) : typical <10 sec

3.2 Summary of Supported Functions

- Tape Deck Commands:

- STOP	a STOP command is sent;
- PLAY,REC	nominal, external varispeed;
- EDIT	EDIT;
- FORW,REW	FWD and REW or controlled FWD and REW sent by interface;
- SHTLF,SHTLR	same as FORW and REW but with lifter off;
- LOC,LOCREL	all locate are performed by the interface using controlled forward and rewind;
- REHEARSE	implemented;
- MUTE	implemented, it can be masked with the DIL switch 81.2;
- EVENT Relays	implemented;
	There is a relay available for the user. The relay can be switched on by the EVON synchronizer command and off by the EVOFF command;

- CONDITIONAL COMMANDS: the timecode triggered execution is possible for the tape deck commands, the relay commands and the audio mute and rehearse commands;

- STATUS Request: The status information are requested and updated through the serial communication link by the interface software. Additional information on the speed is available at the synchronizer via the move pulse connection.

- AUDIO Channel Control: "INPUT SELECT", "MUTE" and "READY/SAVE" of each channel can be controlled individually. Local changes of any status is recognized and transferred to the synchronizer.

  Channel assignments are
  CHANNEL 1 .. 2 = Audio Track 1 .. 2
  CHANNEL 3 = TC Track

- TRANSPARENT Commands: complete ASCII string for commands and answer, no cr/lf added or removed by the interface;

- KEYBOARD DISABLE: implemented.

3.3 DIL-SWITCH Functions

DIL SWITCH SZ81 allows the setting of some general modes.

- Switch 1: RECORD ENABLE
  Defines the polarity of RECEN (see section 3.4)
  OFF: RECORD enabled when
  - low level at RECEN pin
  ON: RECORD enabled when
  - high level at RECEN pin or input open

- Switch 2: AUDIO MUTE
  Allows to suppress MUTE commands for applications with time code recorded on an audio track.
  OFF: MUTE commands are enabled
  ON: no MUTE commands are transmitted to the slave

- Switch 4: TC DELAY UNIT OFF / ON
  The delay unit off the slave machine can be switched off. In this case the delay will be compensated by the synchronizer.
  OFF: Delay unit ON
  ON: Delay unit OFF

  If you use the A812 or A820 as a slave, the "ON" position is recommended. If the timecode is required as reference for any other equipment, switch 4 has to be in OFF position.

All other switches are not used and should be in OFF position.

Default Settings: all switches in OFF position

3.4 Additional Features at the SLAVE CONTROL B Connector

RECEN (PIN 2):
This signal is used to enable/disable the RECORD function with an external hardware. According to DIL-Switch position 1 and the level of the signal RECEN, RECORD commands are passed to the slave or modified to PLAY. (Ref to section 3.3)

REL1 (PIN6), REL2 (PIN7):
A general purpose relay is controlled by EVON/EVOFF commands. The switch REL1/REL2 is closed with the command EVON.

B-REHEA (Pin8), SREHSL (Pin12):
The rehearse mode can be activated by a low level at SREHSL. B-REHR as tally is active when the rehearse mode is switched on (by SREHSL or with a serial command from the synchronizer). This feature is provided for a parallel remote control of REHEARSE.

MVCL (PIN21), MVDR (PIN24):
This output provides buffered movepulse information to supply further synchronizer with master movepulses.

direction MVDR: LOW = forward

MVCL frequency for A812:	64 Hz @ 7.5 ips 128 Hz @ 15 ips 256 Hz @ 30 ips
MVCL frequency for A820:	256 Hz @ 7.5 ips 512 Hz @ 15 ips 1024 Hz @ 30 ips

XVSEN/XVSREF (Pin 5, Pin 3):
An external varispeed circuit can be connected to the TLS.
The two signals are switched to the slave during the OFF mode of the synchronizer.

enable varispeed	XVSENB:	LOW = enabled
reference frequency	XVSREF:	9600 Hz nominal

3.5 LED Diagnostic Display

Three LEDs are situated at the front of the interface board. They provide information about the result of the initial selftest and the online status.

DL 1 2 3 **(front view)**
(# = LED blinking, - = LED off, * = LED on)

- An initialization procedure is executed after reset and the main hardware devices are tested. Any resulting error is signalled with a blinking left LED (DL1, about 1 Hz).
  If all LEDs are blinking, the internal EEPROM of the processor has to be reconfigured. This should only happen if the processor was replaced. In this case the processor should be reconfigured or replaced by one with correct EEPROM configuration.

DL1	DL2	DL3	
#	#	#	Microprocessor 68HC11 has to be reconfigured
#	-	-	CPU-RAM test failed.
#	-	*	RAM test failed.
#	*	-	SSDA test failed.
#	*	*	ACIA test failed.

- If no error was found, DL1 stays dark and the other two LEDs light, if communication with the slave or the synchronizer fails.

DL1	DL2	DL3	
–	*	*	no connection with the synchronizer board
–	*	–	no connection with the SLAVE (ex: remote off)
–	–	*	SLAVE error (ex: slave in echo mode)

- If the left LED is on, a fatal processor error has occurred.
  A reset is necessary to return to operation mode. The interface board should be checked whenever such an error was encountered.

DL1	DL2	DL3	
*	–	–	Fatal SW or HW error (eg ROM defect)
*	–	*	Watch dog error
*	*	–	Clock error
*	*	*	Illegal opcode

3.6 Applications Hints

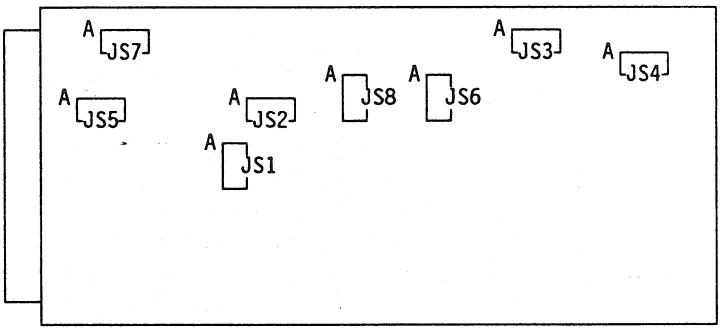
- It is recommended not to use the parallel remote control connector of the slave for the varispeed function when working with the synchronizer. Use the XVS inputs at the synchronizer control B connector. Otherwise conflict between the synchronizer and the varispeed device could occur.
  (Refer to section 3.4 for more information)

- Remote switching of the synchronizer from the slave machine is available.

- If the A812 or A820 is operated as a slave machine only, it will be better to disable the internal delay unit with DIL switch 4. If the switch is ON the delay unit will be switched off automatically and the delay will be compensated by the synchronizer.
  If the machine is providing timecode as master of the system, it is necessary to have a working delay unit. Check DIL switch 2 to be in OFF position for that case.

4 Service Documentation

4.1 Jumper Settings



Functions of jumpers:

	Position AB	Position BC
JS1	Processor in special test mode	Processor in normal expanded mode *
JS2	PE6 input of the processor is LOW	PE6 input of the processor is HIGH *
JS3	Serial output TX/TA connected to MAX232 (RS 232) *	Serial output TX/TA connected to 75176 (RS 422)
JS4	Serial input of 68A50 is connected to MAX232 (RS 232) *	Serial input of 68A50 is connected to 75176 (RS 422)
JS5	IF ground is connected to the slave ground *	No connection between IF ground and slave ground
JS6	Capstan reference output has no pullup resistor	Capstan reference output has a pullup resistor *
JS7	Opto isolated inputs are supplied from the IF *	Opto isolated inputs are supplied from the slave
JS8	Capstan pullup resistor is supplied with 5V (or MVCC if JS7 'AB')	Capstan pullup resistor is supplied with 15V *

* Default setting for STUDER A812/A820

4.2 Signal description, slave connectors

SLAVE CONTROL A:

Pin	Signal	Type	Slave Sig.	Description
1	MGND		+0.0	0.0V from slave
2	-			
3	-			
4	-			
5	CAPEN	I out	SR-VRSPD	capstan varispeed enable (LOW=en)
6	RX/RA		TRANSA	from TRANSA of slave
7	MOVCL	I in	OR-MVCLK	move signal clock from slave
8	TX/TA		RECEIVA	to RECEIVA of slave
9	PAIN5	I in		not used
10	MOVDIR	I in	OR-MVDIR	move signal direction from slave LOW = rewind
11	+5V			5 V IF VCC
12	0.0V		FRMGND	0 V IF GND
13	CAPCL	I out	IR-REFEX	capstan clock, 9600 Hz nominal
14	RB			not used
15	-			
16	-			
17	-			
18	-			
19	PAOUT5	I out		not used
20	-			
21	-			
22	-			
23	-			
24	TB			not used
25	MVCC	+5V	+5V	24 V from slave

signal types:

I out	logic output, active low (open collector, max 30V/0.3A)
I in	logic input, active low, optoisolated (I-low > 10 mA)

SLAVE CONTROL B:

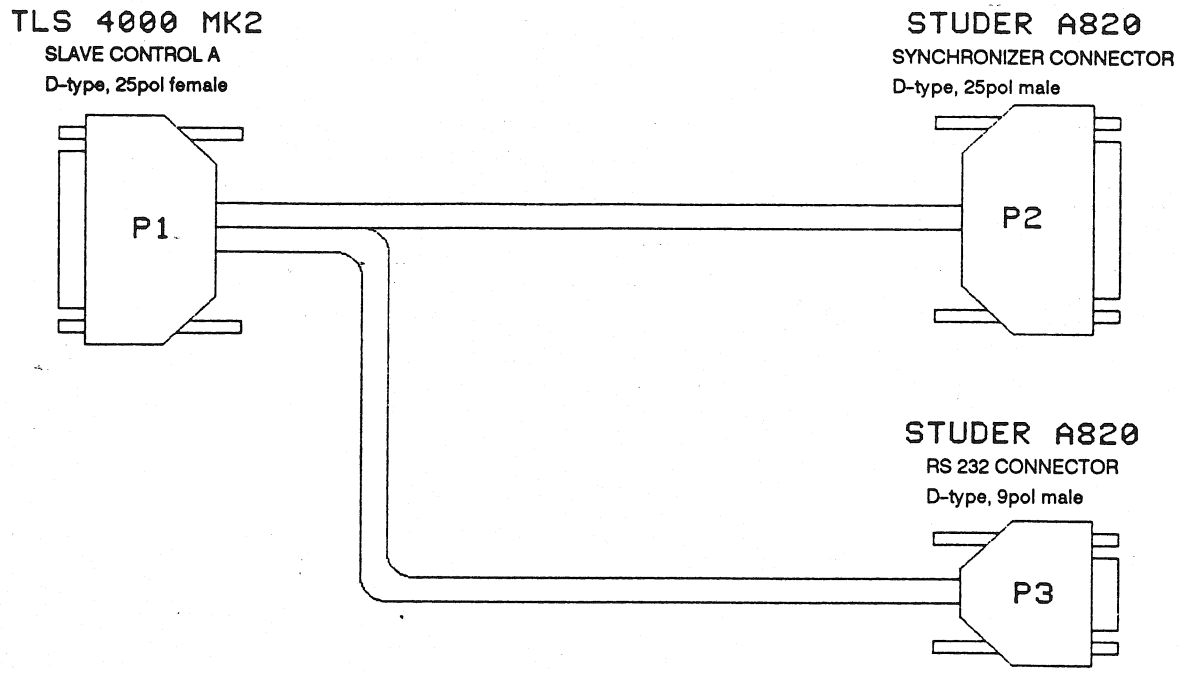
Pin	Signal	Type		Description
1	0.0V			0 V IF GND
2	RECEN/PAIN11	I in		record enable/ safe input (see DIL Switch 81.1)
3	XVSREF/PAIN10	I in		external varispeed frequency
4	-			
5	XVSEN/PAIN9	I in		external varispeed enable
6	REL1			event relay contact 100V/0.3A
7	REL2			event relay contact 100V/0.3A
8	PAOUT6	I out		rehearse on indication
9	-			
10	-			
11	+5V			5.0 V IF VCC
12	PAIN12	I in		rehearsal input
13	-			
14	DC			not used
15	-			
16	-			
17	-			
18	-			
19	-			
20	0.0V			0 V IF GND
21	MVCL	I out		move signal clock (ref sec. 3.4)
22	SCITX			not used
23	SCIRX			not used
24	MVDR	I out		move signal direction (LOW = FORW)
25	0.0V			0 V IF GND

signal types:

I out	logic output, active low (open collector, max 30V/0.3A)
I in	logic input, active low, optoisolated (I-low > 10 mA)

Remark: Schematics → see universal serial IF

4.3 IF Cable Description



P1. 1	MGND	P2. 1
5	CAPEN	5
7	MOVCL	7
10	MOVDIR	10
13	CAPCL	13
25	MVCC	25
	SCREEN	14

P1. 6	RX/RA	P3. 2
8	TX/TA	8
12	0,0V	9
	SCREEN	1

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